PF09K16*
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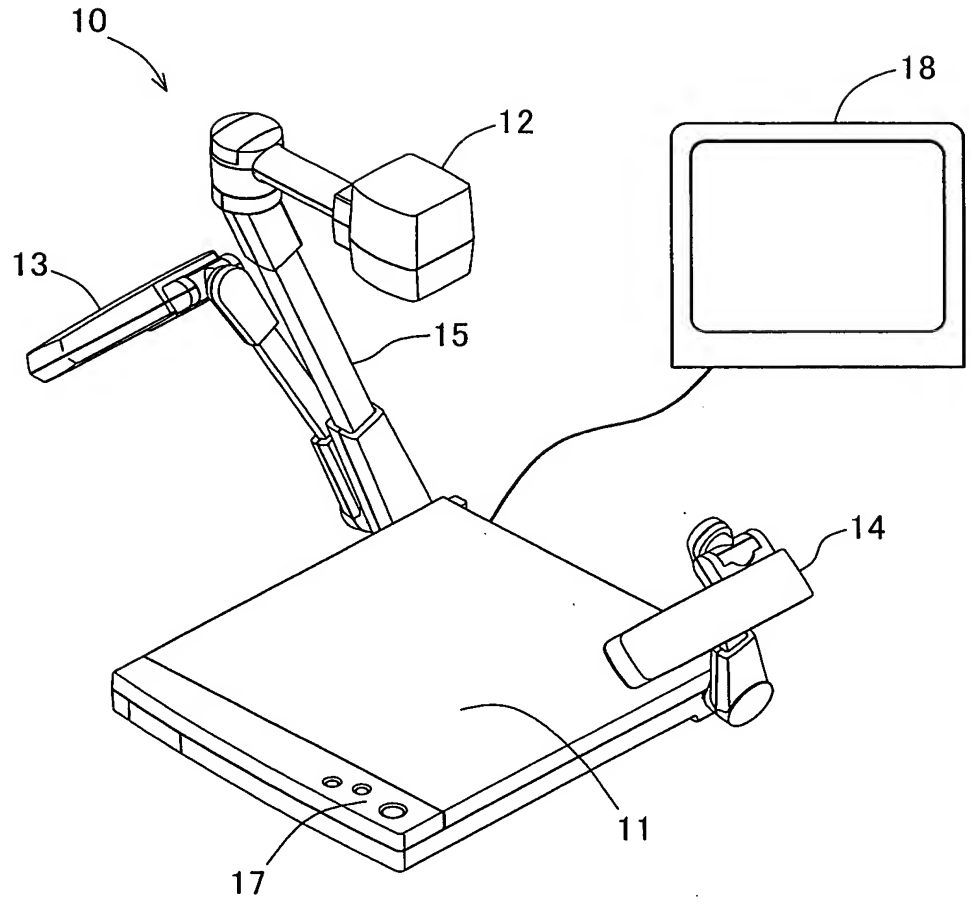
PATENT & TRADEMARK OFFICE

Fig.1



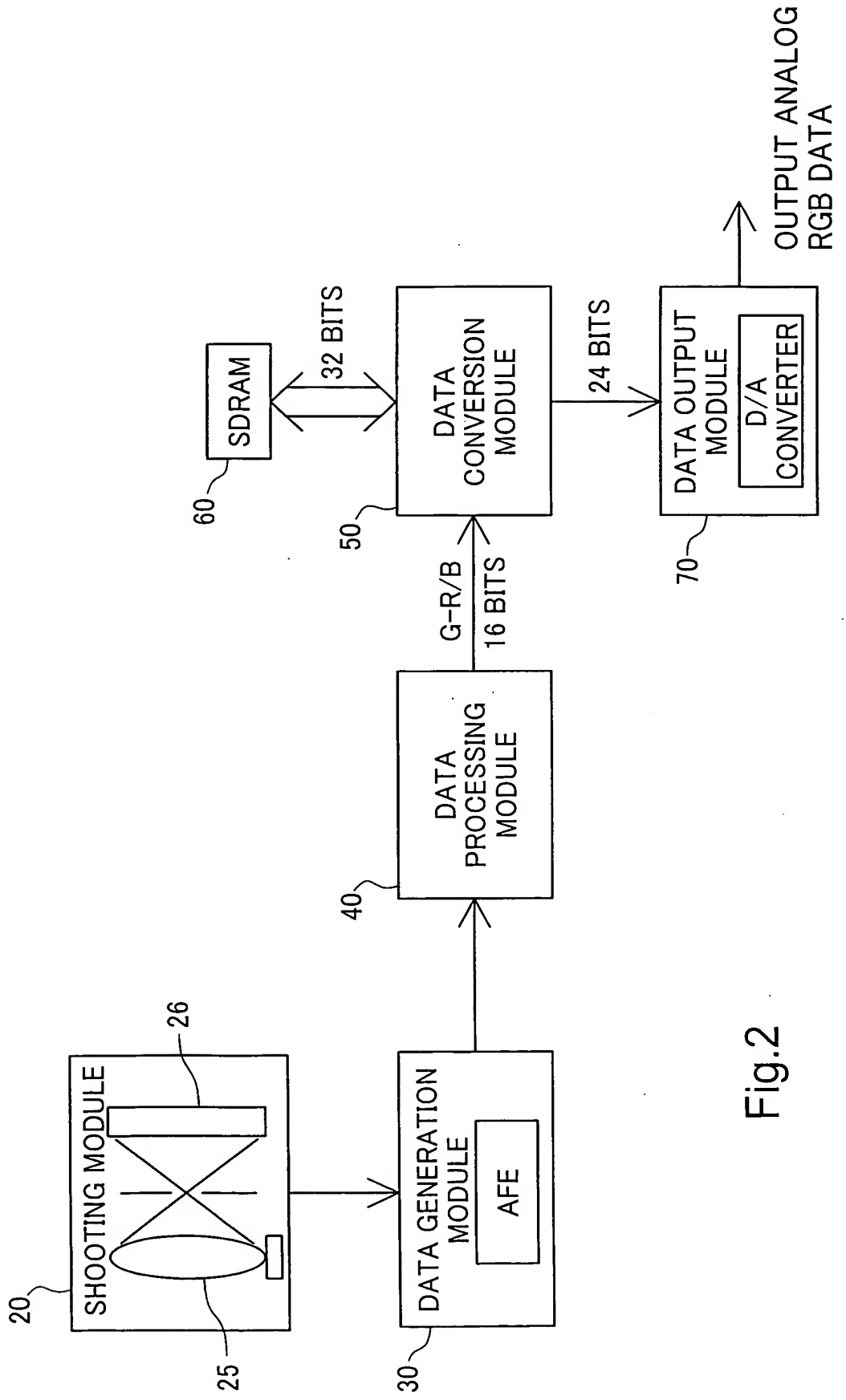

SHOOTING MODULE
20
26
25
DATA GENERATION MODULE
AFE
30
DATA PROCESSING MODULE
40
G-R/B
16 BITS
DATA CONVERSION MODULE
50
SDRAM
60
32 BITS
24 BITS
DATA OUTPUT MODULE
D/A CONVERTER
70
OUTPUT ANALOG RGB DATA

Fig.2

Fig.3

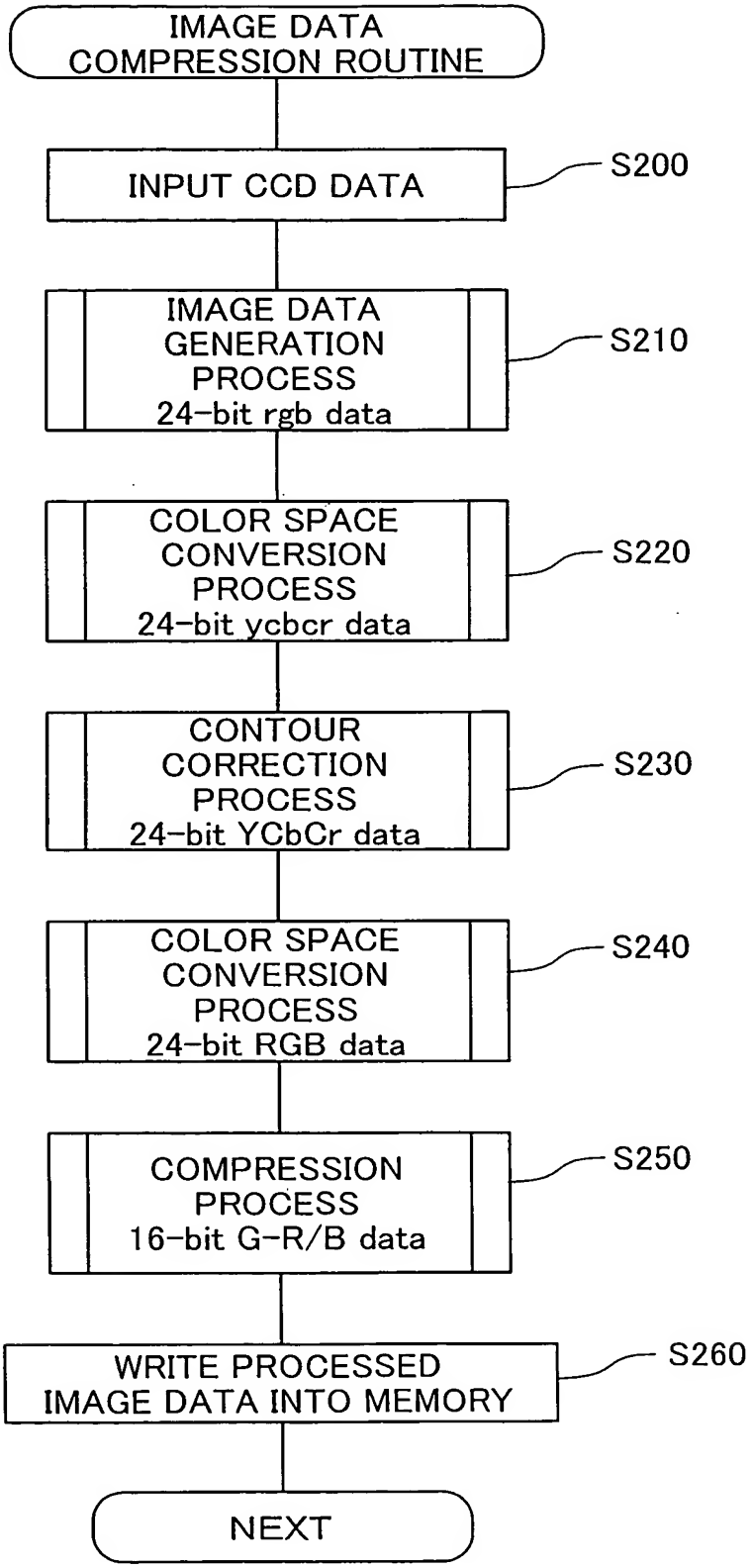


IMAGE DATA COMPRESSION ROUTINE
INPUT CCD DATA
S200
IMAGE DATA GENERATION PROCESS 24-bit rgb data
S210
COLOR SPACE CONVERSION PROCESS 24-bit ycbcr data
S220
CONTOUR CORRECTION PROCESS 24-bit YCbCr data
S230
COLOR SPACE CONVERSION PROCESS 24-bit RGB data
S240
COMPRESSION PROCESS 16-bit G-R/B data
S250
WRITE PROCESSED IMAGE DATA INTO MEMORY
S260
NEXT

Fig.4

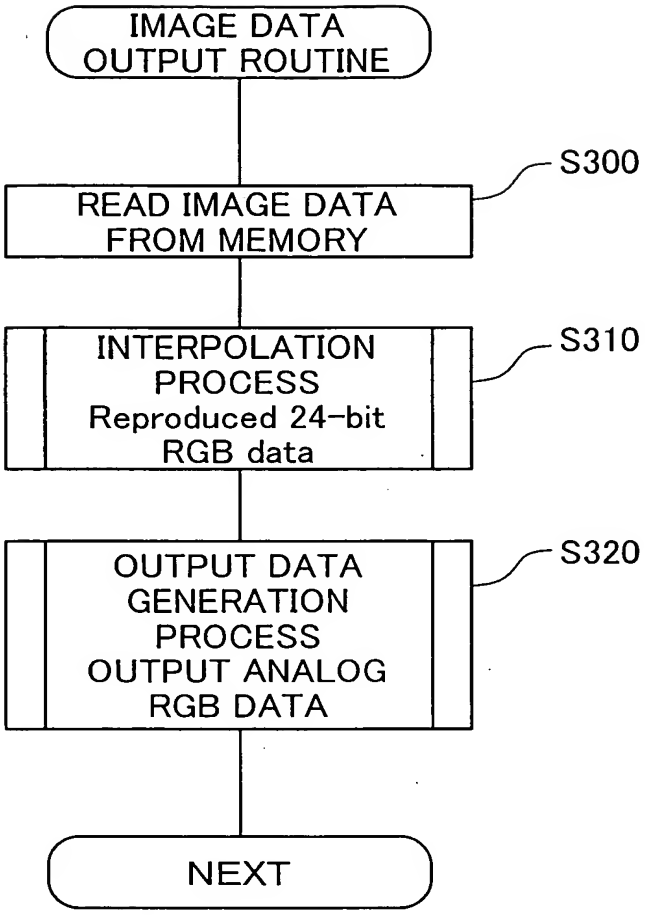


IMAGE DATA OUTPUT ROUTINE
S300
READ IMAGE DATA FROM MEMORY
S310
INTERPOLATION PROCESS Reproduced 24-bit RGB data
S320
OUTPUT DATA GENERATION PROCESS OUTPUT ANALOG RGB DATA
NEXT

r1	r2	r3	r4	r5	r6	r7	r8	r9	r10	r11	r12
g1	g2	g3	g4	g5	g6	g7	g8	g9	g10	g11	g12
b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	b11	b12

Fig.5(a)

y1	y2	y3	y4	y5	y6	y7	y8	y9	y10	y11	y12
cb1	cb2	cb3	cb4	cb5	cb6	cb7	cb8	cb9	cb10	cb11	cb12
cr1	cr2	cr3	cr4	cr5	cr6	cr7	cr8	cr9	cr10	cr11	cr12

Fig.5(b)

Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12
Cb1	Cb2	Cb3	Cb4	Cb5	Cb6	Cb7	Cb8	Cb9	Cb10	Cb11	Cb12
Cr1	Cr2	Cr3	Cr4	Cr5	Cr6	Cr7	Cr8	Cr9	Cr10	Cr11	Cr12

Fig.5(c)

R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Fig.5(d)

G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12
R1	B1	R3	B3	R5	B5	R7	B7	R9	B9	R11	B11

Fig.5(e)

R1	R2´	R3	R4´	R5	R6´	R7	R8´	R9	R10´	R11	R12´
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12
B1	B2´	B3	B4´	B5	B6´	B7	B8´	B9	B10´	B11	B12´

Fig.5(f)